aa

b₃

a₃b₁

 a_2

 b_2

 $\overline{a_3b_0}$ a_2b_0 a_1b_0

 $a_2b_1 a_1b_1 a_0b_1$

a₁

b₁

a₀ x

 b_0

 a_0b_0

Laboratory 3

(Due date: **002/003**: Feb. 20th, **004**: Feb. 21st, **006**: Feb. 22nd)

OBJECTIVES

- ✓ Use the Structural Description on VHDL.
- ✓ Test arithmetic circuits on an FPGA.

VHDL CODING

✓ Refer to the <u>Tutorial: VHDL for FPGAs</u> for a list of examples.

FIRST ACTIVITY (100/100)

DESIGN PROBLEM

• The figure depicts a 2's complement array multiplier for two 4-bit signed numbers. It is based on the basic unsigned multiplier with some adjustments.



PROCEDURE

• Vivado: Complete the following steps:

- Create a new Vivado Project. Select the corresponding Artix-7 FPGA device (e.g.: the XC7A50T-1CSG324 FPGA device for the Nexys A7-50T).
- ✓ Write the VHDL code for this signed array multiplier. <u>Synthesize</u> your code.
 - Use the Structural Description: Create a separate .vhd file for the Full Adder, the Processing Unit (PU), the flipped Processing Unit (PUn) and the top file (Array Multiplier).
- ✓ Write the VHDL testbench to test the circuit for all possible cases (256 cases). Use 'for loop'.
- ✓ Perform <u>Functional Simulation</u> and <u>Timing Simulation</u> of your design. **Demonstrate this to your TA**.
 - Your simulation might need more time than Vivado Simulator's default (1 us). For example, to add 5 us, you can go to the TCL console and type: run 5 us.
 - Note that you can represent your data as signed (2C) integers (use $Radix \rightarrow Signed Decimal$).

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- ✓ I/O Assignment: Generate the XDC file associated with your board.
 - Suggestion:

Board pin names	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
Signal names in code	A ₃	A_2	A_1	A ₀	B ₃	B ₂	B ₁	B ₀	P ₇	P ₆	P ₅	P ₄	P ₃	P_2	P ₁	P ₀

- The board pin names are used by all the listed boards (Nexys A7-50T/A7-100T, Basys 3, Nexys 4/DDR). The I/Os listed here are all active high.
- ✓ Generate and download the bitstream on the FPGA and perform testing: use a sample of representative cases (e.g.: 8 cases) from your testbench. Demonstrate this to your TA.

SUBMISSION

- Submit to Moodle (an assignment will be created):
 - \checkmark The lab sheet (<u>as a .pdf</u>) signed off by the TA (or instructor).
 - (<u>As a .zip file</u>) the six generated files: VHDL code (4 files), VHDL testbench, and XDC file. **DO NOT submit the whole Vivado Project**.
 - Your .zip file should only include one folder. Do not include subdirectories.
 It is strongly recommended that all your design files, testbench, and
 - It is strongly recommended that all your design files, testbench, and constraints file be located in a single directory. This will allow for a smooth experience with Vivado.
 - You should only submit your source files AFTER you have demoed your work. Submission of work files without demoing will be assigned <u>NO CREDIT</u>.

lab3	
	Design files
	Testbench file
lab3.xdc	Constraints file

TA signature: _____

Date: _____